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REMARKS

Claims 6-29, 31, and 33-42 are pending in the application. Claims 8-25 and 33-42 are subject to a restriction requirement.

Claims 6, 7, 26-32 have been elected for prosecution and stand rejected.

Withdrawal of the objection to the drawings under 37 C.F.R. § 1.83(a) is requested. Claims 6 corresponds to Fig. 3, and claims 7 and 26 correspond to Fig. 1. Claim 26 has been amended to make it clear that the bit dispenser is in fact a bit data separator which is shown in the figure.

Withdrawal of the rejection of claims 26-29 under 35 U.S.C. § 112, is requested. Claims 26-29 have been rewritten to avoid the concern noted in the Office Action.

Withdrawal of the rejection of claims 6 and 7 under 35 U.S.C. § 112, is requested. Claims 6 and 7 have been amended to make it clear how the first and second data are coded and the particular arrangement of first and second data bits in the memory cells.

A provisional double patenting rejection is noted. The judicially created doctrine of double patenting can be cured by a terminal disclaimer which the Applicants will consider once allowable subject matter is indicated in the application.

Withdrawal of the rejection of claims 26, 29 and 31 under 35 U.S.C. § 102(e) as being anticipated by Baldi (U.S. Pat. No. 5,761,222), is requested. The present invention as defined in claims 26, 29 and 31 requires that at least a bit of an N-order of first data bits and at least a bit of an M-order of second data bits be stored in one of the cells, similar to that shown in Fig. 3. This feature is also contained in claim 6, which is not rejected under 35 U.S.C. § 102. Since the reference does not appear to disclose this particular feature of the amended claims, the reference cannot anticipate or suggest the subject matter of these claims.

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It is to be noted that Baldi (U.S. Pat. No. 5,761,222) is directed to a apparatus and method for making error corrections to digital data. The system disclosed in the reference utilizes two memories, wherein error correction data is stored separately from actual data. Error correction data is available to correct the actual data when needed. This is distinctly different from the present invention which is directed to an apparatus which stores data bits in accordance with a specific format, to thereby facility reading out of the data.

Withdrawal of the rejection of claims 27, 28, 30 and 32 under 35 U.S.C. § 103, as being unpatentable over Baldi (U.S. Pat. No. 5,761,222), is requested. Claims 27 and 28 have been amended, and claims 30 and 32 have been cancelled. Claims 27 and 28 have been amended to include all the subject matter of claim 26. As was noted with respect to claim 26, the device includes a controller which enters a first data, having a first plurality of data bits and the second data stream comprising a second plurality of data bits, where each have been coded. In accordance with amended claim 26, a bit data separator separates the first and second data bits to store at least a bit of an Nth-order of the first data bits and at least a bit of an Mth-order of the second data bits in one of the cells. This particular limitation does not appear to be in the Baldi reference. As noted previously, Baldi is directed to a system and method for storing data correction codes in a second memory, which can be used to restore data containing errors in a first memory. The reference fails to disclose the foregoing limitation and therefore can neither render obvious or anticipate the subject matter of rejected claims 27 and 28, which are dependent on parent claim 26.

In view of the foregoing, favorable reconsideration is believed to be in order.

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The Commissioner is hereby authorized to charge any deficiency with the filing of this paper to our Deposit Account No. 22-0185, under Order No. 21737-00013-US from which the undersigned is authorized to draw.

Dated: 11/26/03   Respectfully submitted,

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